REMARKS

Claims 1-24 were pending. The Applicants have amended claims 1, 21, and 22, , leaving claims 1-24 for the Examiner's consideration. No new matter has been added. In the Office Action, the Examiner has rejected claims 1-24 under 35 U.S.C. §112(1), 35 U.S.C. §102(e), and 35 U.S.C. §103(a). The Applicants respectfully traverse these rejections.

I. Rejection of claims 1-5, 10-15, and 21-24 under 35 U.S.C. §112

The Examiner has rejected claims 1-5, 10-15, and 22-24 on the grounds that the specification fails to provide an enabling description of the claim term "configuration inputs selectively coupled with each of the plurality of configuration blocks and adapted to communicate configuration data." The Examiner states that the specification is unclear as to how the configuration inputs are selectively coupled.

The Applicants have amended claims 1 and 22 to remove the term "selectively." This amendment renders this rejection of claims 1 and 22 moot. Claim 10 does not recite the term "selectively." Thus, it is unclear to the Applicants how these grounds for rejection apply to claim 10. The Applicants respectfully request that this rejection either be withdrawn or clarified to identify the pertinent element of claim 10.

Claim 21 has been amended to clarify the elements of "command word" and "data word." The Applicants respectfully request the withdraw of this rejection.

II. Rejection of claim 1 under 35 U.S.C. §102

The Examiner has rejected claim 1 in view of the admitted prior art disclosed in the specification and figures 1 and 2. In the Office Action, the Examiner asserts that the clock input 220 in figure 2 is analogous to the "plurality of command inputs adapted to independently enable loading of at least one of the plurality of configuration blocks." The Applicants respectfully disagree.

As shown in figure 2, the clock input 220 is connected to all of the configuration blocks. According the Examiner, all of the configuration blocks are loaded simultaneously in

response to the clock signal. Because all of the configuration blocks of the prior art are loaded with the same configuration data simultaneously in response to a single clock signal, the prior art cannot load data into some of the configuration blocks while leaving the remaining configuration blocks unchanged. Thus, the clock input 220 does not enable configuration blocks to be loaded independently of each other and is not analogous to a command input "adapted to independently enable loading of at least one of the plurality of configuration blocks," as recited by claim 1.

Moreover, the Applicants note that this rejection of claim 1 contradicts the Examiner's rejection of claim 1 under 35 U.S.C. §112(1). In rejecting claim 1 under 35 U.S.C. §112, the Examiner is alleging that the specification does not disclose one element of claim 1. However, in rejecting claim 1 under 35 U.S.C. §102(a) in view of admitted prior art in the specification, the Examiner is alleging that the specification discloses all of the elements of claim 1. Both of these cannot be true. If the specification does not provide an enabling disclosure of every element of claim 1, then the admitted prior art in the specification cannot anticipate this claim.

Therefore, the Applicants respectfully submit that claim 1 and its dependents are patentable over the admitted prior art.

III. Rejection of claims 1-5, 10-15, and 20-24 under 35 U.S.C. §102

The Examiner has rejected claims 1-5, 10-15, and 20-24 as anticipated by Young et. al., U.S. Patent No. 6,526,557 ("Young"). Claim 1 recites in part:

a plurality of command inputs adapted to independently enable loading of at least one of the plurality of configuration blocks, wherein the plurality of configuration blocks are adapted to simultaneously load configuration data via the plurality of configuration inputs in response to the plurality of command inputs.

The Applicants respectfully submit that Young does not disclose or suggest at least this element.

Young discloses "an FPGA architecture and method [that] enables partial reconfiguration of selected configurable logic blocks (CLBs)." Configurable logic blocks are

programmable logic blocks that implement the desired function of the FPGA. (Col. 1:55-60). The "configuration of the logic and the connection between line segments is controlled by a configuration memory, into which a configuration is loaded for enabling the logic and interconnect lines to perform a desired function." (Col. 1:59-63). According to Young, "a frame of configuration data is fed serially into a shift register, then shifted in parallel to an addressed column of configuration memory cells." (Col. 1:66-7:2). Thus, the programmable device of Young receives configuration data using a register, and then transfers configuration data from the register to configuration memory cells.

Young enables selective reconfiguration of configuration memory cells using one of two approaches. "One approach is to control the input signals being applied to memory cells in such a way that certain ones of the memory cells addressed by a common address line are selectively programmed while other are not." (Col. 3:61-64.). A second approach modifies the configuration memory cells of the FPGA to include "an extra set of address lines in addition to the existing address lines." (Col. 6:15-16). These extra address lines "[enable] selection of individual CLBs so that a particular CLB can be reconfigured without affecting other CLBs. (Col. 6:30-32).

In both of the approaches of Young, the configuration memory cells are modified to enable selective access. Young does not disclose or suggest using a register, rather than the configuration memory cells, to enable selective data loading.

Claim 1 recites "a plurality of command inputs adapted to independently enable loading of at least one of the plurality of configuration blocks." As noted in the specification, "a configuration word register includes an N number of configuration blocks." (Paragraph [0021]). In light of the Applicants' definition of configuration blocks, claim 1 clearly refers to a register, not configuration memory cells. Because Young does not disclose or suggest any means of using a register to selectively load configuration data, the Applicants respectfully submit that claim 1 and its dependents are patentable over Young.

The Examiner cites various portions of Young as disclosing configuration blocks as recited by claim 1. However, all of these cited portions refer to configuration logic blocks (CLBs), which Young defines as logic blocks controlled by configuration memory cells. These

citations include Col. 4, lines 4-10, Col. 1, lines 63-66, Col. 5, lines 58-62, and Col. 6. lines 16-27 and 44-55. The CLBs of Young are not part of a configuration word register. (Configurable logic blocks are programmable logic blocks that implement the desired function of the FPGA. The "configuration of the logic and the connection between line segments is controlled by a configuration memory, into which a configuration is loaded for enabling the logic and interconnect lines to perform a desired function." (Col. 1:55-63).)

The Applicants respectfully submit that claims 10 and 22, as well as their respective dependent claims, are patentable over Young for similar reasons as set forth with respect to claim 1.

IV. Rejection of claims 6-9 and 16-19 under 35 U.S.C. §103

The Examiner has rejected claims 6-9 and 16-19 as unpatentable over Young in view of Lesea et al., U.S. Patent No. 6,496,971 ("Lesea"). The Applicants respectfully submit that these claims are patentable over the cited references at least by virtue of their dependence on patentable independent claims.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

The Applicants invite the Examiner to contact the undersigned if he believes a telephone conference would expedite the prosecution of this application.

Respectfully submitted,

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Attachments
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